SECTION 8
ELECTRICAL SPECIFICATIONS

This section contains electrical specifications and associated timing information for the MC68010.

8.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC68010 MC68010C	T_A	T_L to T_H 0 to 70 −40 to 85	°C
Storage Temperature	T_{stg}	−55 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

8.2 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Rating
Thermal Resistance			
Ceramic	θ_{JA}	30	°C/W
Plastic with Heat Spreader		30	
Type B Chip Carrier		50	
Type C Chip Carrier		50	

8.3 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = T_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The curve shown in Figure 8-1 gives the graphic solution to these equations for the specification power dissipation of 1.50 and 1.75 watts over the ambient temperature range of −55°C to 125°C using a θ_{JA} of 45°C/W for the ceramic (L suffix) package.

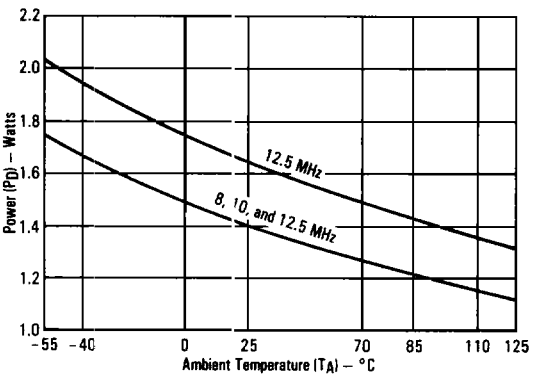


Figure 8-1. MC68010 Power Dissipation (P_D) vs Ambient Temperature (T_A)

8.4 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%; V_{SS} = 0 Vdc; T_A = T_L to T_H; see Figures 8-2, 8-3, and 8-4)

Characteristic		Symbol	Min	Max	Unit
Input High Voltage		V_{IH}	2.0	V_{CC}	V
Input Low Voltage		V_{IL}	V_{SS} − 0.3	0.8	V
Input Leakage Current @ 5.25 V	$\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, CLK, $\overline{IPL0}$-$\overline{IPL2}$, $\overline{VPA}$	I_{in}	–	2.5	μA
	$\overline{HALT}$, $\overline{RESET}$		–	20	
Three-State (Off State) Input Current @ 2.4 V/0.4 V	$\overline{AS}$, A1-A23, D0-D15, FC0-FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	I_{TSI}	–	20	μA
Output High Voltage (I_{OH} = −400 μA)	E*	V_{OH}	V_{CC} − 0.75	–	V
	E**, $\overline{AS}$, A1-A23, $\overline{BG}$, D0-D15, FC0-FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$		2.4	–	
Output Low Voltage		V_{OL}			V
(I_{OL} = 1.6 mA)	$\overline{HALT}$		–	0.5	
(I_{OL} = 3.2 mA)	A1-A23, $\overline{BG}$, FC0-FC2		–	0.5	
(I_{OL} = 5.0 mA)	$\overline{RESET}$		–	0.5	
(I_{OL} = 5.3 mA)	E, $\overline{AS}$, D0-D15, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$		–	0.5	
Power Dissipation (See Section 9)***		P_D	–	–	W
Capacitance (V_{in} = 0 V T_A = 25°C; Frequency = 1 MHz)****		C_{in}	–	20.0	pF

*With external pullup resistor of 1.1 kΩ.

**Without external pullup resistor.

***During normal operation instantaneous V_{CC} current requirements may be as high as 1.5 A.

****Capacitance is periodically sampled rather than 100% tested.

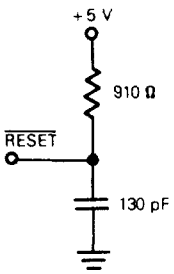


Figure 8-2. $\overline{\text{RESET}}$ Test Load

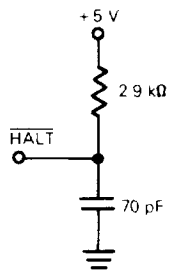


Figure 8-3. $\overline{\text{HALT}}$ Test Load

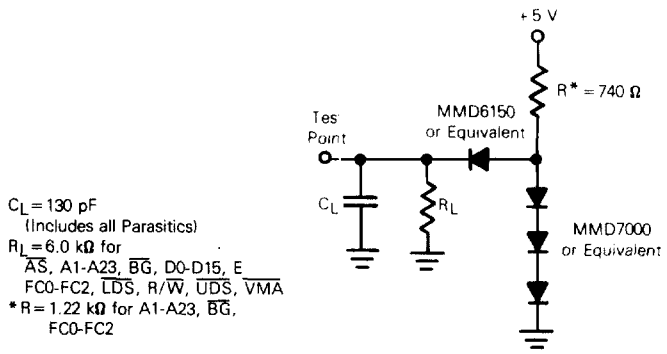


Figure 8-4. Test Loads

8.5 AC ELECTRICAL SPECIFICATIONS — CLOCK INPUT (See Figure 8-5)

Characteristic	Symbol	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation	f	2.0	8.0	2.0	10.0	4.0	12.5	MHz
Cycle Time	t_{cyc}	125	500	100	500	80	250	ns
Clock Pulse Width	t_{CL} t_{CH}	55 55	250 250	45 45	250 250	35 35	125 125	ns
Rise and Fall Times	t_{Cr} t_{Cf}	– –	10 10	– –	10 10	– –	5 5	ns

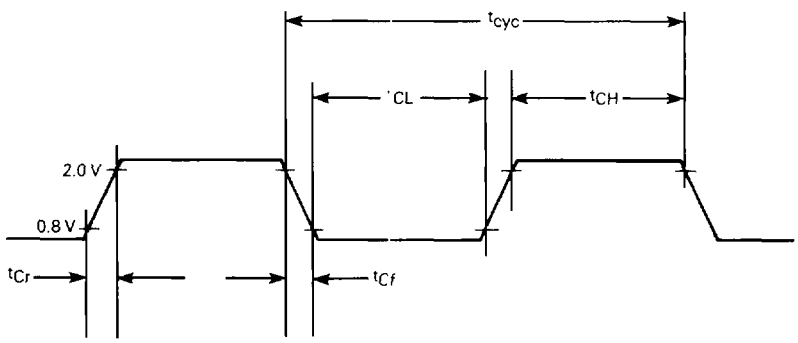


Figure 8-5. Clock Input Timing Diagram

8.6 AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

(V_{CC} = 5.0 Vdc ±5%; V_{SS} = 0 Vdc; $T_A = T_L$ to T_H; see Figures 8-6 and 8-7)

Num.	Characteristic	Symbol	8 MHz		10 MHz		12.5 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Clock Period	t_{cyc}	125	500	100	500	80	250	ns
2	Clock Width Low	t_{CL}	55	250	45	250	35	125	ns
3	Clock Width High	t_{CH}	55	250	45	250	35	125	ns
4	Clock Fall Time	t_{Cf}	–	10	–	10	–	5	ns
5	Clock Rise Time	t_{Cr}	–	10	–	10	–	5	ns
6	Clock Low to Address Valid	t_{CLAV}	–	70	–	55	–	55	ns
6A	Clock High to FC Valid	t_{CHFCV}	–	70	–	60	–	55	ns
7	Clock High to Address Data High Impedance (Maximum)	t_{CHAZx}	–	80	–	70	–	60	ns
8	Clock High to Address/FC Invalid (Minimum)	t_{CHAZn}	0	–	0	–	0	–	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Low (Maximum)	t_{CHSLx}	–	60	–	55	–	55	ns
10	Clock High to $\overline{AS}$, $\overline{DS}$ Low (Minimum)	t_{CHSLn}	0	–	0	–	0	–	ns
11[2]	Address Valid to $\overline{AS}$, $\overline{DS}$ (Read) Low/$\overline{AS}$ (Write)	t_{AVSL}	30	–	20	–	0	–	ns
11A[2]	FC Valid to $\overline{AS}$, $\overline{DS}$ (Read) Low/$\overline{AS}$ (Write)	t_{FCVSL}	60	–	50	–	40	–	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ High	t_{CLSH}	–	70	–	55	–	50	ns
13[2]	$\overline{AS}$, $\overline{DS}$ High to Address/$\overline{FC}$ Invalid	t_{SHAZ}	30	–	20	–	10	–	ns
14[2]	$\overline{AS}$, $\overline{DS}$ Width Low (Read)/$\overline{AS}$ (Write)	t_{SL}	240	–	195	–	160	–	ns
14A[2]	$\overline{DS}$ Width Low (Write)	–	115	–	95	–	80	–	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width High	t_{SH}	150	–	105	–	65	–	ns
16	Clock High to $\overline{AS}$, $\overline{DS}$ High Impedance	t_{CHSZ}	–	80	–	70	–	60	ns
17[2]	$\overline{AS}$, $\overline{DS}$ High to R/$\overline{W}$ High	t_{SHRH}	40	–	20	–	10	–	ns
18[1]	Clock High to R/$\overline{W}$ High (Maxmum)	t_{CHRHx}	–	70	–	60	–	60	ns
19	Clock High to R/$\overline{W}$ High (Minimum)	t_{CHRHn}	0	–	0	–	0	–	ns
20[1]	Clock High to R/$\overline{W}$ Low	t_{CHRL}	–	70	–	60	–	60	ns
20A[2]	AS Low to R/$\overline{W}$ Valid	t_{ASRV}	–	20	–	20	–	20	ns
21[2]	Address Valid to R/$\overline{W}$ Low	t_{AVRL}	20	–	0	–	0	–	ns
21A[2]	FC Valid to R/$\overline{W}$ Low	t_{FCVRL}	60	–	50	–	30	–	ns
22[2]	R/$\overline{W}$ Low to $\overline{DS}$ Low (Write)	t_{RLSL}	80	–	50	–	30	–	ns
23	Clock Low to Data Out Valid	t_{CLDO}	–	70	–	55	–	55	ns
24	Clock High to R/$\overline{W}$, $\overline{VMA}$ High Impedance	t_{CHRZ}	–	80	–	70	–	60	ns
25[2]	$\overline{DS}$ High to Data Out Invalid	t_{SHDO}	30	–	20	–	15	–	ns
26[2]	Data Out Valid to $\overline{DS}$ Low (Write)	t_{DOSL}	30	–	20	–	15	–	ns
27[5]	Data In to Clock Low (Setup Time)	t_{DICL}	15	–	10	–	10	–	ns
27A	Late $\overline{BERR}$ Low to Clock Low (Setup Time)	t_{BELCL}	45	–	45	–	45	–	ns
28[2]	$\overline{AS}$, $\overline{DS}$ High to $\overline{DTACK}$ High	t_{SHDAH}	0	245	0	190	0	150	ns
29	$\overline{DS}$ High to Data Invalid (Hold Time)	t_{SHDI}	0	–	0	–	0	–	ns
30	$\overline{AS}$, $\overline{DS}$ High to $\overline{BERR}$ High	t_{SHBEH}	0	–	0	–	0	–	ns
31[2,5]	$\overline{DTACK}$ Low to Data Valid (Setup Time)	t_{DALDI}	–	90	–	65	–	50	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	$t_{RHr, f}$	0	200	0	200	0	200	ns
33	Clock High to $\overline{BG}$ Low	t_{CHGL}	–	70	–	60	–	50	ns
34	Clock High to $\overline{BG}$ High	t_{CHGH}	–	70	–	60	–	50	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
36	$\overline{BR}$ High to $\overline{BG}$ High	t_{BRHGH}	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	t_{GALGH}	1.5	3.0	1.5	3.0	1.5	3.0	Clk. Per.

– Continued

8.6 AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (Continued)

(V_{CC}=5.0 Vdc ±5%; V_{SS}=0 Vdc; T_A=T_L to T_H; see Figures 8-6 and 8-7)

Num.	Characteristic	Symbol	8 MHz		10 MHz		12.5 MHz		Unit
			Min	Max	Min	Max	Min	Max	
37A	$\overline{BGACK}$ Low to $\overline{BR}$ High (to Prevent Rearbitration)	t_{BGKBR}	20	–	20	–	20	–	ns
38	$\overline{BG}$ Low to Bus High Impedance (wtih $\overline{AS}$ High)	t_{GLZ}	–	80	–	70	–	60	ns
39	$\overline{BG}$ Width High	t_{GH}	1.5	–	1.5	–	1.5	–	Clk. Per.
40	Clock Low to $\overline{VMA}$ Low	t_{CLVML}	–	70	–	70	–	70	ns
41	Clock Low to E Transition	t_{CLC}	–	70	–	55	–	45	ns
42	E Output Rise and Fall Time	$t_{Er, f}$	–	25	–	25	–	25	ns
43	$\overline{VMA}$ Low to E High	t_{VMLEH}	200	–	150	–	90	–	ns
44	$\overline{AS}$, $\overline{DS}$ High to $\overline{VPA}$ High	t_{SHVPH}	0	120	0	90	0	70	ns
45	E Low to Address/$\overline{VMA}$/$\overline{FC}$ Invalid	t_{ELAI}	30	–	10	–	10	–	ns
46	$\overline{BGACK}$ Width	t_{BGL}	1.5	–	1.5	–	1.5	–	Clk. Per.
47[5]	Asynchronous Input Setup Time	t_{ASI}	20	–	20	–	20	–	ns
48[2,3]	$\overline{DTACK}$ Low to $\overline{BERR}$ Low	t_{DALBEL}	–	80	–	55	–	35	ns
49	E Low to $\overline{AS}$, $\overline{DS}$ Invalid	t_{ELSI}	−80	–	−80	–	−80	–	ns
50	E Width High	t_{EH}	450	–	350	–	280	–	ns
51	E Width Low	t_{EL}	700	–	550	–	440	–	ns
52	E Extended Rise Time	t_{CIEHX}	–	80	–	80	–	80	ns
53	Data Hold from Clock High	t_{CHDO}	0	–	0	–	0	–	ns
54	Data Hold from E Low (Write)	t_{ELDOZ}	30	–	20	–	15	–	ns
55	R/$\overline{W}$ to Data Bus Impedance Change	t_{RLDO}	30	–	20	–	10	–	ns
56[4]	$\overline{HALT}$/$\overline{RESET}$ Pulse Width	t_{HRPW}	10	–	10	–	10	–	Clk. Per.

NOTES:

1. For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the values given in these columns.
2. Actual value depends on clock period.
3. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (#47).
4. For power up, the MPU must be held in $\overline{RESET}$ state for 100 ms to allow stabilization of on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the system.
5. If the asynchronous setup time (#47) requirements are satisfied, the $\overline{DTACK}$-low to data setup time (#31) and $\overline{DTACK}$-low to $\overline{BERR}$-low setup time (#48) requirements can be ignored. The data must only satisfy the data-in to clock-low setup time (#27) for the following clock cycle, $\overline{BERR}$ must only satisfy the late-$\overline{BERR}$-ow to clock-low setup time (#27A) for the following clock cycle.

Timing diagrams (Figures 8-6 and 8-7) are located on foldout pages 1 and 2 at the end of this document.

8.7 AC ELECTRICAL SPECIFICATIONS — MC68010 TO M6800 PERIPHERAL CYCLES

(V_{CC}=5.0 Vdc ±5%, V_{SS}=0 Vdc, T_A=T_L to T_H, refer to Figures 8-8 and 8-9)

Num.	Characteristic	Symbol	8 MHz		10 MHz		12.5 MHz		Unit
			Min	Max	Min	Max	Min	Max	
23	Clock Low to Data Out Valid	t_{CLDO}	–	70	–	55	–	55	ns
24	Clock High to R/$\overline{W}$, $\overline{VMA}$ High Impedance	t_{CHRZ}	–	80	–	70	–	60	ns
27	Data In to Clock Low (Setup Time)	t_{DICL}	15	–	10	–	10	–	ns
40	Clock Low to $\overline{VMA}$ Low	t_{CLVML}	–	70	–	70	–	70	ns
41	Clock Low to E Transition	t_{CLC}	–	70	–	55	–	45	ns
42	E Output Rise and Fall Time	$t_{Er, Ef}$	–	25	–	25	–	25	ns
43	$\overline{VMA}$ Low to E High	t_{VMLEH}	200	–	150	–	90	–	ns
44	$\overline{AS}$, $\overline{DS}$ High to $\overline{VPA}$ High	t_{SHVPH}	0	120	0	90	0	70	ns
45	E Low to Address/$\overline{VMA}$/FC Invalid	t_{ELAI}	30	–	10	–	10	–	ns
47	Asynchronous Input Setup Time	t_{AS1}	20	–	20	–	20	–	ns
49	E Low to $\overline{AS}$, $\overline{DS}$ Invalid	t_{ELSI}	−80	–	−80	–	−80	–	ns
50	E Width High	t_{EH}	450	–	350	–	280	–	ns
51	E Width Low	t_{EL}	700	–	550	–	440	–	ns
52	E Extended Rise Time	t_{CIEHX}	–	80	–	80	–	80	ns
54	Data Hold from E Low (Write)	t_{ELDOZ}	30	–	20	–	15	–	ns

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

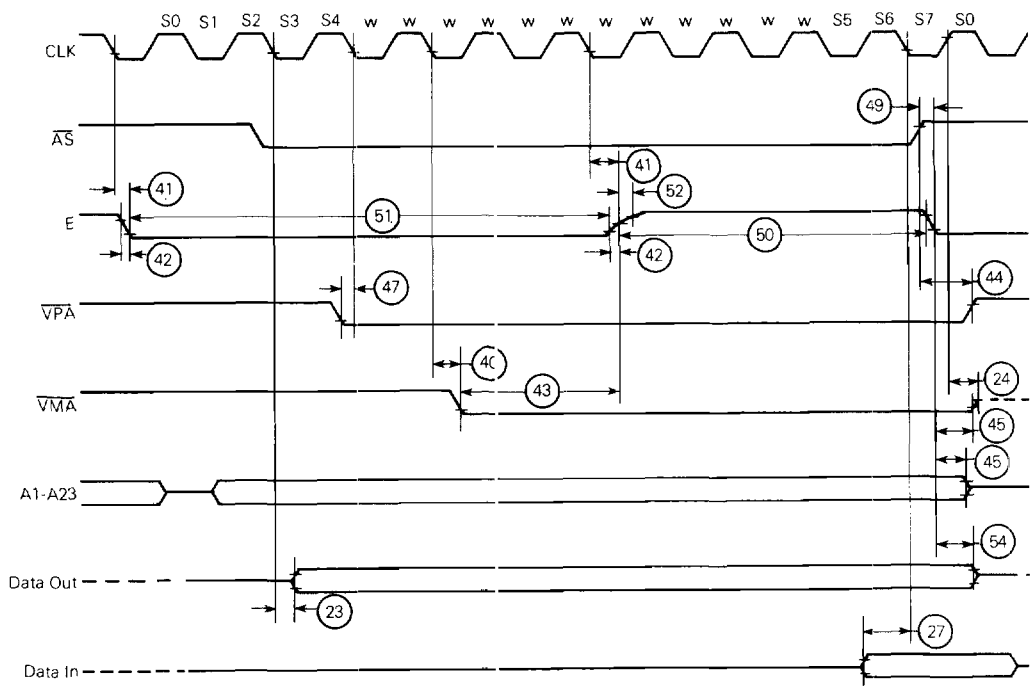


Figure 8-8. MC68010 to M6800 Peripheral Timing Diagram — Best Case

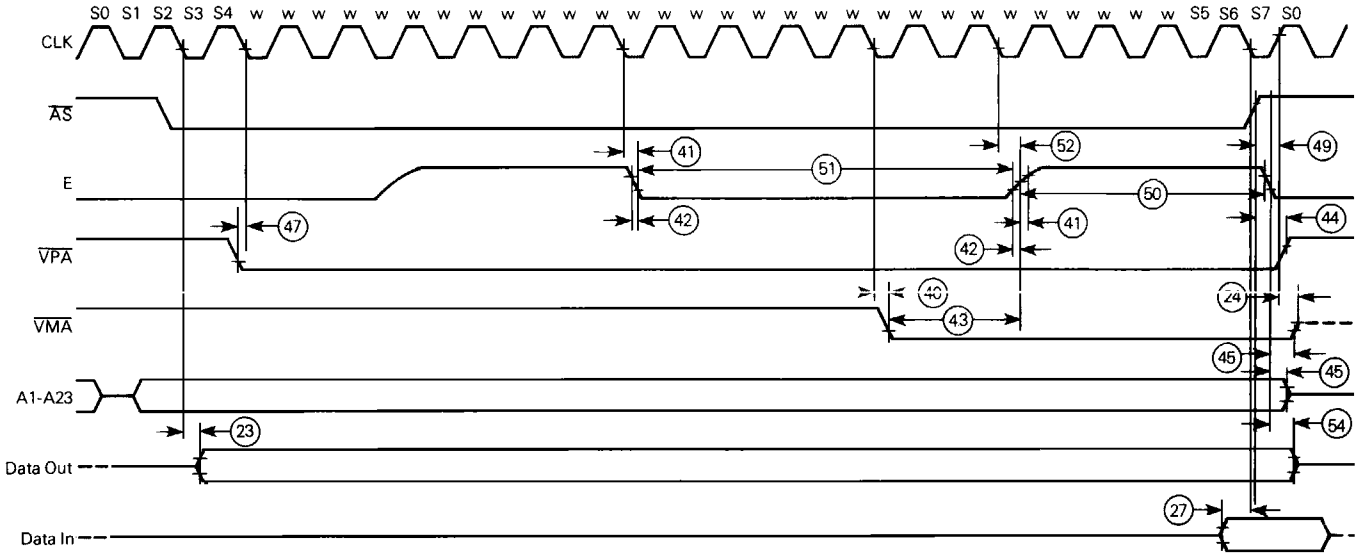


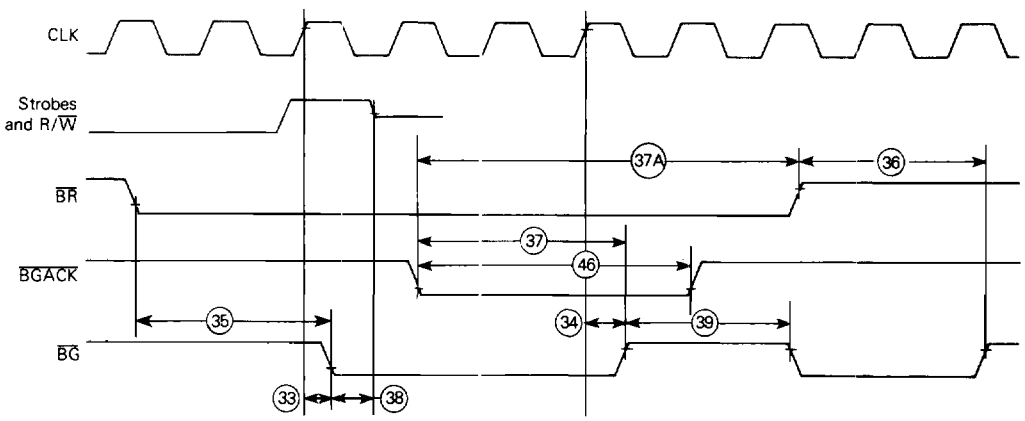
Figure 8-9. MC68010 to M6800 Peripheral Timing Diagram — Worst Case

8.8 AC ELECTRICAL SPECIFICATIONS — BUS ARBITRATION

(V_{CC} = 5.0 Vdc ±5%; V_{SS} = 0 Vdc; $T_A = T_L$ to T_H; see Figure 8-10)

Num.	Characteristic	Symbol	8 MHz		10 MHz		12.5 MHz		Unit
			Min	Max	Min	Max	Min	Max	
33	Clock High to $\overline{BG}$ Low	t_{CHGL}	–	70	–	60	–	50	ns
34	Clock High to $\overline{BG}$ High	t_{CHGH}	–	70	–	60	–	50	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
36	$\overline{BR}$ High to $\overline{BG}$ High	t_{BRHGH}	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	t_{GALGH}	1.5	3.0	1.5	3.0	1.5	3.0	Clk. Per.
37A	$\overline{BGACK}$ Low to $\overline{BR}$ High (to Prevent Rearbitration)	t_{BGKBR}	20	–	20	–	20	–	ns
38	$\overline{BG}$ Low to Bus High Impedance (with AS High)	t_{GLZ}	–	80	–	70	–	60	ns
39	$\overline{BG}$ Width High	t_{GH}	1.5	–	1.5	–	1.5	–	Clk. Per.
46	$\overline{BGACK}$ Width	t_{BGL}	1.5	–	1.5	–	1.5	–	Clk. Per.

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



NOTES:

1. Setup time for the asynchronous inputs $\overline{BERR}$, $\overline{BGACK}$, $\overline{BIi}$, $\overline{DTACK}$, $\overline{IPL0}$-$\overline{IPL2}$, and $\overline{VPA}$ guarantees their recognition at the next falling edge of the clock.
2. Waveform measurements for all inputs and outputs are specified at: logic high = 2.0 volts, logic low = 0.8 volts.

Figure 8-10. Bus Arbitration Timing